Rule 1.126

34.

~~36.~~ (New) The computer system of claim ~~35~~ 33, wherein the configuration device comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

Rule 1.126

35.

~~37.~~ (New) The computer system of claim ~~36~~ 34, wherein the plurality of different interfaces comprises:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

Rule 1.126

36.

~~38.~~ (New) The computer system of claim ~~37~~ 35, wherein the memory device is a flash memory and the test interface is a standard flash memory interface and the operation interface is a proprietary interface.

Rule 1.126

37.

~~39.~~ (New) The computer system of claim ~~35~~ 33, wherein the memory device is a BIOS memory.

REMARKS

Entry of the above-listed amendment prior to examination of the above-referenced case on the merits is respectfully requested. Claims 1-20 have been

cancelled. New claims 21-39 have been added. It is respectfully submitted that no new matter has been introduced by this preliminary amendment.

Applicant respectfully submits that claim 21 is not anticipated by U.S. Patent No. 5,841,715 of Farmwald, et al. ("Farmwald").

Claim 21 recites:

> A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes.

Claim 21 is not anticipated by Farmwald because Farmwald discloses memory devices that each have only a single interface. The memory devices of Farmwald include a ROM memory 12 with device interface 161, a DRAM memory 13 with device interface 161, and a DRAM memory 14 with device interface 161. Device interface 161 is the same interface common to all of the memory devices. Device interface 161 consists of an electrical interface, address comparison circuitry and timing registers, and a DRAM column access path (Farmwald, col. 21, lines 9-26). These parts represent the three main parts of device interface 161, however, and are not different interfaces within device interface 161. In particular, Farmwald discloses that "each memory device contains only a *single bus interface* with no other signal pins." (Farmwald, col. 3, line 53 to col. 4, line 5, emphasis added; and Figure 2). Nothing in Farmwald teaches memory devices wherein each memory device has a plurality of different interfaces.

Even if one were to interpret the computer system of Figure 2 of Farmwald as a memory device containing multiple interfaces within it, such an interpretation of the disclosure of Farmwald would still not anticipate claim 21 because the interfaces of Farmwald are identical interfaces and not different interfaces, as previously discussed. Nothing in Farmwald discloses "a memory device comprising a plurality of different interfaces to operate the memory

device in a plurality of different modes," as recited in claim 21. Therefore, claim 21 is not anticipated by Farmwald.

For reasons similar to those given with respect to claim 21, applicant respectfully submits that claim 28 is not anticipated by Farmwald.

Given that claims 29-33 depend from claim 28, applicant submits that claims 29-33 are also not anticipated by Farmwald.

For reasons similar to those given with respect to claim 21, applicant respectfully submits that claim 34 is not anticipated by Farmwald.

Given that claims 35-39 depend from claim 34, applicant submits that claims 35-39 are also not anticipated by Farmwald.

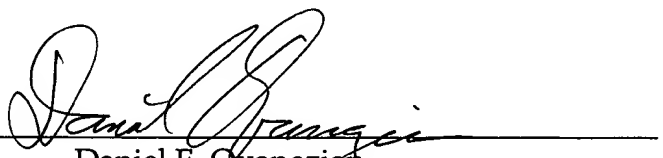
In conclusion, applicants respectfully submit that in view of the amendments and arguments set forth herein, the claims are in condition for allowance.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8/10, 2001



Daniel E. Ovanezian
Reg. No. 41,236

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8598

MARKED-UP VERSION SHOWING CHANGES

IN THE SPECIFICATION

The paragraph beginning at page 5, line 19 and ending at page 5, line 25 has been amended as follows:

The MCH 65 controls operations between processor 60 and memory devices, for examples, a graphics controller 62 and a random access memory (RAM) 64. The ICH 70 controls operations between processor 60 and input/output (I/O) devices, for examples, a keyboard (KBD) 73 and a mouse 74. The ICH 70 also controls operations between processor 60 and peripheral devices, for examples, a drive 71 and a modem 72. In another embodiment, the MCH 65 and the ICH 70 may be integrated into a single component.

The paragraph beginning at page 8, line 7 and ending at page 8, line 22 has been amended as follows:

Figure 3 illustrates one embodiment of an interface. In one embodiment, the memory device 350 is configured with a standard flash interface 352 for testing device functionality at wafersort. The standard flash interface 352 includes 20 address pads 301-308, and 313-324; control pads 309, 311-312, and 336-338; configuration pad 339; supply pads 310, and 329-331; data (DQ) pads 325-328, and 332-335; and no connect (NC) pad 340. The control pads 309, 311-312, and 336-338 [339] are used for control operations of the memory device 350, for examples, chip enable, output enable, reset, and status. Configuration pad 339 is used to select between the test interface and the other interfaces used, for example, during the programming and operation modes of memory device 350. During wafersort testing at the component manufacturer, data is loaded into and

read from the memory device 350 on data pads 325-328 to test for defects. The 20 pad address configuration allows for accessing the memory device 350 in one cycle because the address information can be loaded in parallel, thereby allowing data to be read on the same cycle.

The paragraph beginning at page 9, line 6 and ending at page 9, line 17 has been amended as follows:

Figure 4 illustrates one embodiment of another interface. In one embodiment, interface 454 is a programming interface that may be used in programming the memory device with firmware. As previously discussed, programming is performed after the memory device 350 is assembled into a package and ready for assembly onto the motherboard 61 of Figure 1. During this time, memory device 450 [350] is programmed with low level code to enable the startup of computer system 75 of Figure 1. Configuration pad 402 is bonded out in the packaged memory device 450 for selecting between the programming interface 454 and another interface, for example, a test interface 352 of Figure 3. In one embodiment, configuration pad 439 (used to select the test interface while in test mode) is not connected in the packaged memory device 450 as the test interface is no longer required.

The paragraph beginning at page 9, line 18 and ending at page 10, line 2 has been amended as follows:

Access to the memory device 450 when assembled in a package may be accomplished through the programming interface 454. In one embodiment, the programming interface 454 is no longer used after the computer system 75 of Figure 1 is manufactured. In another embodiment, the programming interface may be used at a later time to reprogram the memory device 450 to operate with

new technologies. Use of a programming interface 454 having a standard protocol may allow motherboard manufacturers to program the memory device 450 without requiring memory manufacturers to disclose a proprietary interface to motherboard manufacturers.

The paragraph beginning at page 10, line 3 and ending at page 10, line 13 has been amended as follows:

In one embodiment, the programming interface 454 is an Address/Address multiplexer (A/A mux) interface having 11 address pads, 407 and 415-424; control pads 409, 411, 412, and 436-438; configuration pads 402 and 439; supply pads 410 and 429-431; data pads (DQ) 425-428 and 432-435; and no connect (NC) pads 401 [410], 403-406, 408, 413-414, and 440. Data pads 425-428 are used to transfer firmware code data into memory locations (not shown) of memory device 450. The firmware code is programmed into particular memory locations of memory device 450 using address pads 407 and 415-424. Memory data addressing and storage is well known in the art. Accordingly, a detailed description of the memory device's internal components and operation is not provided herein.

The paragraph beginning at page 11, line 3 and ending at page 11, line 12 has been amended as follows:

Although[,] a second cycle is required to load the memory device with a full address, the A/A Mux interface 454 is suited for use in programming operations where the additional time of using two cycles may not significantly contribute to the total cycle time of programming operations. The memory device[s] 450 features that are dropped off due to use of a smaller pin count package may include, for example[s], locking. Locking is a protection feature

that prevents the memory device from being intentionally or inadvertently overwritten. Because the A/A mux interface 454 is usually used only for programming, the additional circuit logic for locking may not be required.

The paragraph beginning at page 11, line 13 and ending at page 11, line 23 has been amended as follows:

Figure 5 illustrates yet another embodiment of an interface. In one embodiment, a third interface 556 [536] is an operation interface. Operation interface 556 is used during operation of memory device 550 in computer system 75 on motherboard 61 of Figure 1. Operation interface 556 includes multiplexed address/data (A/DQ) pads 525-528; configuration pads 502 and 539; supply pads 510[,] and 529-531; control pads 511-512, 519-520, and 537-538; identification (ID) pads 521-524; clock (CLK) pad 509; and[,] no[t] connect[ed] pads 501, 503-508, 513-518, 532-536, and 540. A/DQ pads 525-528 may be multiplexed to function as both address and data pads. CLK pad 509 may be used to synchronize timing operations of memory device 550 with other chipset components on motherboard 61 of Figure 1.

The paragraph beginning at page 11, line 24 and ending at page 12, line 8 has been amended as follows:

Configuration pad 539 is used to select between the operation interface 556 and the programming interface 454 [456] of Figure 4. The configuration pad 539 is coupled to interface selection circuitry that functions to switch between different memory device circuitry that is coupled to a particular I/O pad. For example, a particular I/O pad connected to control circuitry during operation of the memory device may be switched to address circuitry when programming the device. As such, additional dedicated I/O pads are not needed for programming

operations. This eliminates the need for a larger pin count package required when a memory device contains dedicated pads for programming operations.

The paragraph beginning at page 12, line 14 and ending at page 19, line 7 has been amended as follows:

A memory device having multiple interfaces enables use of a proprietary interface during device operation while allowing programming of the device through a programming interface that may be released to motherboard manufacturers. Having separate interfaces allows a memory device manufacturer to withhold a device interface specification from tool enabling customers such as BIOS programmers.

The paragraph beginning at page 12, line 20 and ending at page 13, line 7 has been amended as follows:

Figure 6 illustrates one embodiment of interface selection circuitry. Memory device 650 includes selection circuitry coupled to the pads of the device for switching between multiple device interfaces. In one embodiment, the selection circuitry coupled to pad 609, for example, includes control multiplexer 680 and drivers 684, 686, and 688. In one embodiment, drivers 684, 686, and 688 [686] may be coupled to different control function circuitry within memory device 650. For example, driver 686 [684] may be coupled to chip enable circuitry 687 used during testing; driver 688 [686] may be coupled to row / column address selection circuitry 689 to toggle between a low and high order address during programming; [,] and driver 684 [686] may be coupled to clock circuitry 685 used during in-system device operations. Two configuration lines 639

and 602 are coupled to control multiplexer 680 and used to select between the multiple interfaces containing the different device functions.

IN THE CLAIMS

Claims 21-38 have been added.